UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/779,808	02/18/2004	Paul Anthony Gilkerson	550-525	6826

23117 7590 04/21/2006

NIXON & VANDERHYE, PC
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER	
FENNEMA, ROBERT E	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/779,808	GILKERSON, PAUL ANTHONY	
	Examiner	Art Unit	
	Robert E. Fennema	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 July 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 are pending.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because it exceeds 150 words.

Correction is required. See MPEP § 608.01(b).

Drawings

4. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because they are informal. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the additional pipeline stages as disclosed in Claims 5, 9, 15, and 19 must be shown or the feature(s) canceled from the claim(s). Also, the Address Generation paths as disclosed in Claims 1-21 must be shown or the feature(s) cancelled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Information Disclosure Statement

6. Applicant is reminded of their duty to disclose information material to patentability as set forth in the MPEP § 1.56, such as copending applications.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 5, 9, 15, and 19 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claimed invention of adding a pipeline stage in a further address generation path to increase generation speed of a first generation path has not been adequately disclosed to enable one of ordinary skill in the art to make the invention without undue experimentation. Given that the only way that adding a pipeline stage can increase generation speed is by adding a pipeline stage to break up a critical path, it has not been disclosed where or how to add this stage to allow one of ordinary skill in the art to make the disclosed invention. Appropriate correction or clarification is required.

Double Patenting

9. Applicant is advised that should claim 1 be found allowable, claim 21 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-4, 6-8, 10-14, 16-18, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Furber.

11. As per Claim 1, Furber teaches: A data processing apparatus, comprising:

a processor operable to execute a stream of instructions (Page 387, the AMULET 3);

a prefetch unit operable to prefetch instructions from a memory prior to sending those instructions to the processor for execution (Page 387), the prefetch unit being operable to receive from the memory simultaneously a plurality of prefetched instructions from sequential addresses in memory (Page 387, it can fetch two Thumb instructions), and being operable to detect whether any of those prefetched instructions are an instruction flow changing instruction, and based thereon to output a fetch

address for a next instruction to be prefetched by the prefetch unit (Page 382, where it says it modifies the predicted control flow to the predicted target address. Page 387 says that the prefetch unit in the AMULET3 functions similar to the jump trace buffer shown on 382, but to support the multiple instructions, and that a "hit" indicates that it is a branch instruction); and

address generation logic within the prefetch unit and operable, for a selected prefetched instruction that is detected to be said instruction flow changing instruction, to determine a target address to be output as the fetch address (Pages 382-383), the address generation logic having a first address generation path operable to determine the target address if the selected prefetched instruction is a first prefetched instruction in said plurality (Page 388), and at least one further address generation path operable to determine the target address if the selected prefetched instruction is one of the other prefetched instructions in said plurality, the first prefetched instruction being earlier in said stream than said other prefetched instructions (Page 388), the first address generation path being arranged to generate the target address more quickly than the at least one other address generation path (Page 388, the first path takes priority); whereby, in the event that the first prefetched instruction is said selected prefetched instruction, the prefetch unit is operable to output the associated target address as the fetch address earlier than if one of said other prefetched instructions is said selected prefetched instruction (Page 388, the first path takes priority).

12. As per Claim 2, Furber teaches: A data processing apparatus as claimed in claim 1, further comprising:

prediction logic operable to predict, for a prefetched instruction whose execution is conditional, whether that conditional prefetched instruction will be executed by the processor (Pages 382-383);

in the event that the first prefetched instruction is said selected prefetched instruction and its execution is conditional, the prefetch unit being operable to output the associated target address as the fetch address if the prediction logic predicts that the first prefetched instruction will be executed by the processor (Pages 382-383).

13. As per Claim 3, Furber teaches: A data processing apparatus as claimed in claim 1, wherein the prefetch unit associates a different priority level with each of the plurality of prefetched instructions, the first prefetched instruction having the highest priority level, and if more than one of the plurality of prefetched instructions is detected to be said instruction flow changing instruction, the prefetch unit is operable to determine as said selected prefetched instruction the prefetched instruction having the higher priority level from those prefetched instructions detected to be said instruction flow changing instruction, whereby the target address associated with that selected prefetched instruction is output as the fetch address (Page 388).

14. As per Claim 4, Furber teaches: A data processing apparatus as claimed in claim 1, wherein the address generation logic is operable to generate the target address for

the first prefetched instruction in a same clock cycle as the prefetch unit detects that that first prefetched instruction is said instruction flow changing instruction (Page 382).

15. As per Claim 6, Furber teaches: A data processing apparatus as claimed in claim 1, wherein the at least one further address generation path comprises a single further address generation path used to determine the target address for any prefetched instructions other than said first prefetched instruction (Pages 387-388).

16. As per Claim 10, Furber teaches: A data processing apparatus as claimed in claim 1, wherein if none of the plurality of prefetched instructions is said instruction flow changing instruction, the prefetch unit is operable to generate the fetch address by incrementing a previous fetch address output by the prefetch unit (Page 382, figure 14.6).

17. As per Claim 11, Furber teaches: A method of operating a data processing apparatus to determine a target address for an instruction flow changing instruction, the data processing apparatus having a processor operable to execute a stream of instructions (Page 387, the AMULET 3), and a prefetch unit operable to prefetch instructions from a memory prior to sending those instructions to the processor for execution (Page 387), and to output a fetch address for a next instruction to be prefetched from the memory (Page 382, where it says it modifies the predicted control flow to the predicted target address. Page 387 says that the prefetch unit in the

AMULET3 functions similar to the jump trace buffer shown on 382, but to support the multiple instructions, and that a "hit" indicates that it is a branch instruction), the method comprising the steps of:

(a) receiving from the memory simultaneously a plurality of prefetched instructions from sequential addresses in memory (Page 387, it can fetch two Thumb instructions);

(b) detecting whether any of those prefetched instructions are an instruction flow changing instruction (Page 382, where it says it modifies the predicted control flow to the predicted target address. Page 387 says that the prefetch unit in the AMULET3 functions similar to the jump trace buffer shown on 382, but to support the multiple instructions); and

(c) for a selected prefetched instruction that is detected to be said instruction flow changing instruction, determining a target address to be output as the fetch address (Pages 382-383) by performing one of the steps of:

(c)(1) employing a first address generation path to determine the target address if the selected prefetched instruction is a first prefetched instruction in said plurality (Page 388); or

(c)(2) employing at least one further address generation path to determine the target address if the selected prefetched instruction is one of the other prefetched instructions in said plurality (Page 388); the first prefetched instruction being earlier in said stream than said other prefetched instructions, and the first address generation

path being arranged to generate the target address more quickly than the at least one other address generation path (Page 388, the first path takes priority); and

(d) outputting as the fetch address the target address generated at step (c); whereby, in the event that the first prefetched instruction is said selected prefetched instruction, the prefetch unit is operable to output the associated target address as the fetch address earlier than if one of said other prefetched instructions is said selected prefetched instruction (Page 388, the first path takes priority).

18. As per Claim 12, Furber teaches: A method as claimed in claim 11, further comprising the step of:

employing prediction logic to predict, for a prefetched instruction whose execution is conditional, whether that conditional prefetched instruction will be executed by the processor (Pages 382-383);

in the event that the first prefetched instruction is said selected prefetched instruction and its execution is conditional, the prefetch unit being operable to output the associated target address as the fetch address if the prediction logic predicts that the first prefetched instruction will be executed by the processor (Pages 382-383).

19. As per Claim 13, Furber teaches: A method as claimed in claim 11, further comprising the steps of:

associating a different priority level with each of the plurality of prefetched instructions, the first prefetched instruction having the highest priority level (Page 388);

if more than one of the plurality of prefetched instructions is detected to be said instruction flow changing instruction, determining as said selected prefetched instruction for said step (c) the prefetched instruction having the higher priority level from those prefetched instructions detected to be said instruction flow changing instruction (Page 388);

whereby at said step (d) the target address associated with that selected prefetched instruction is output as the fetch address (Page 388).

20. As per Claim 14, Furber teaches: A method as claimed in claim 11, wherein at said step (c)(1) the target address for the first prefetched instruction is generated in a same clock cycle that, during said step (b), that first prefetched instruction is detected as said instruction flow changing instruction (Page 382).

21. As per Claim 16, Furber teaches: A method as claimed in claim 11, wherein the at least one further address generation path comprises a single further address generation path used at said step (c)(2) to determine the target address for any prefetched instructions other than said first prefetched instruction (Pages 387-388).

22. As per Claim 20, Furber teaches: A method as claimed in claim 11, wherein if none of the plurality of prefetched instructions is determined at said step (b) to be said instruction flow changing instruction, the method further comprises the step of:

generating the fetch address by incrementing a previous fetch address output by the prefetch unit, and outputting that fetch address at said step (d) (Page 382, figure 14.6).

23. As per Claim 21, Furber teaches: A prefetch unit for a data processing apparatus that has a processor operable to execute a stream of instructions (Page 387, the AMULET 3), the prefetch unit being operable to prefetch instructions from a memory prior to sending those instructions to the processor for execution (Page 387), the prefetch unit being operable to receive from the memory simultaneously a plurality of prefetched instructions from sequential addresses in memory (Page 387, it can fetch two Thumb instructions), and being operable to detect whether any of those prefetched instructions are an instruction flow changing instruction, and based thereon to output a fetch address for a next instruction to be prefetched by the prefetch unit (Page 382, where it says it modifies the predicted control flow to the predicted target address. Page 387 says that the prefetch unit in the AMULET3 functions similar to the jump trace buffer shown on 382, but to support the multiple instructions, and that a "hit" indicates that it is a branch instruction), the prefetch unit comprising:

address generation logic operable, for a selected prefetched instruction that is detected to be said instruction flow changing instruction, to determine a target address to be output as the fetch address (Pages 382-383), the address generation logic having a first address generation path operable to determine the target address if the selected prefetched instruction is a first prefetched instruction in said plurality (Page 388), and at

least one further address generation path operable to determine the target address if the selected prefetched instruction is one of the other prefetched instructions in said plurality (Page 388), the first prefetched instruction being earlier in said stream than said other prefetched instructions, the first address generation path being arranged to generate the target address more quickly than the at least one other address generation path (Page 388, the first path takes priority);

whereby, in the event that the first prefetched instruction is said selected prefetched instruction, the prefetch unit is operable to output the associated target address as the fetch address earlier than if one of said other prefetched instructions is said selected prefetched instruction (Page 388, the first path takes priority).

Claim Rejections - 35 USC § 103

24. The following is á quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. Claims 7-8 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furber, in view of Hara (USPN 5,848,269).

26. As per Claim 7, Furber teaches: A data processing apparatus as claimed in claim 1, wherein the prefetch unit comprises decode logic operable to detect whether any of

the plurality of prefetched instructions are said instruction flow changing instruction (Pages 382-383), but fails to explicitly teach:

the decode logic further being operable to decode from each prefetched instruction detected to be said instruction flow changing instruction an immediate value to be input to the address generation logic.

While Furber teaches a prefetch unit to detect whether there is an instruction flow changing instruction using a branch prediction unit, and outputting a target address, it is not explicitly taught that the branch prediction unit can handle branches with immediate values. However, Hara teaches a branch prediction mechanism, which can be used for effectively calculating branch targets, without adding excessive hardware (Column 5, Lines 18-24), capable of effectively predicting without a correlating past history (Column 5, Lines 1-5), which has a method for predicting branches with an immediate value, and outputting a target address (Column 8, Lines 44-63, Column 19, Line 58 – Column 20, Line 4, also see Figure 15). Given that branches with immediate targets exist and can be encountered in the instruction stream, and given a need to handle them in Furber's invention, one of ordinary skill in the art at the time the invention was made would have recognized the advantage of using a branch prediction unit such as Hara's, to take advantage of handling immediate values in a branch, while minimizing extra hardware, and being able to effectively predict branches even without correlation with past results.

27. As per Claim 8, Hara teaches: A data processing apparatus as claimed in claim 7, wherein the address generation logic comprises adder logic operable to determine

the target address for the selected prefetched instruction by adding the associated input immediate value to the address of that selected prefetched instruction (Figure 15, and Column 19, Line 58 – Column 20, Line 4).

28. As per Claim 17, Furber teaches: A method as claimed in claim 11, wherein the prefetch unit comprises decode logic operable at said step (b) to detect whether any of the plurality of prefetched instructions are said instruction flow changing instruction (Pages 382-383), but fails to explicitly teach: the method further comprising the step of:

employing the decode logic to decode from each prefetched instruction detected to be said instruction flow changing instruction an immediate value for use in said step (c).

While Furber teaches a prefetch unit to detect whether there is an instruction flow changing instruction using a branch prediction unit, and outputting a target address, it is not explicitly taught that the branch prediction unit can handle branches with immediate values. However, Hara teaches a branch prediction mechanism, which can be used for effectively calculating branch targets; without adding excessive hardware (Column 5, Lines 18-24), capable of effectively predicting without a correlating past history (Column 5, Lines 1-5), which has a method for predicting branches with an immediate value, and outputting a target address (Column 8, Lines 44-63, Column 19, Line 58 – Column 20, Line 4, also see Figure 15). Given that branches with immediate targets exist and can be encountered in the instruction stream, and given a need to handle them in Furber's invention, one of ordinary skill in the art at the time the invention was made would have

recognized the advantage of using a branch prediction unit such as Hara's, to take advantage of handling immediate values in a branch, while minimizing extra hardware, and being able to effectively predict branches even without correlation with past results.

29. As per Claim 18, Hara teaches: A method as claimed in claim 17, wherein at said step (c) the target address for the selected prefetched instruction is determined by adding the associated immediate value to the address of that selected prefetched instruction (Figure 15, and Column 19, Line 58 – Column 20, Line 4).

30. Claims 5 and 15 are rejected under 35 U.S.C. 103(a), as being unpatentable over Furber, in view of Patterson et al. (herein Patterson).

31. As per Claim 5, Furber teaches: A data processing apparatus as claimed in claim 1, wherein predetermined logic is shared between the first address generation path and the at least one further address generation path (Page 387, a memory), and

a pipeline stage is provided in the at least one further address generation path in order to increase speed of generation of the target address by the first address generation path.

However, Patterson teaches that pipelining a processor, or adding stages of a pipeline, will reduce CPI, and reduce clock cycle time (increasing the rate at which the clock runs) (Page A-3), which would then speed up execution of the first address path, due to the increased clock rate. Given this advantage, it would have been obvious to

one of ordinary skill in the art at the time the invention was made to pipeline a processing path that took one long clock cycle, to increase the clock rate for other paths, and apply it to Furber's invention.

32. As per Claim 15, Furber teaches: A method as claimed in claim 11, wherein predetermined logic is shared between the first address generation path and the at least one further address generation path (Page 387, a memory), but fails to teach:

and the method further comprises the step of:

providing a pipeline stage in the at least one further address generation path in order to increase speed of generation of the target address by the first address generation path.

However, Patterson teaches that pipelining a processor, or adding stages of a pipeline, will reduce CPI, and reduce clock cycle time (increasing the rate at which the clock runs) (Page A-3), which would then speed up execution of the first address path, due to the increased clock rate. Given this advantage, it would have been obvious to one of ordinary skill in the art at the time the invention was made to pipeline a processing path that took one long clock cycle, to increase the clock rate for other paths, and apply it to Furber's invention.

33. Claims 5 and 15 are rejected under 35 U.S.C. 103(a), as being unpatentable over Furber and Hara, in view of Patterson.

34. As per Claim 9, Furber and Hara teach: A data processing apparatus as claimed in claim 8, wherein the adder logic is shared between the first address generation path and the at least one further address generation path (Hara, Column 19, Line 58 – Column 20, Line 4 discloses the adder, and Furber, Page 388 discloses that one path takes priority, meaning only one target can be output at a time, meaning the adder must be shared), but fails to explicitly teach:

and a pipeline stage is provided in the at least one further address generation path in order to increase speed of generation of the target address by the first address generation path.

However, Patterson teaches that pipelining a processor, or adding stages of a pipeline, will reduce CPI, and reduce clock cycle time (increasing the rate at which the clock runs) (Page A-3), which would then speed up execution of the first address path, due to the increased clock rate. Given this advantage, it would have been obvious to one of ordinary skill in the art at the time the invention was made to pipeline a processing path that took one long clock cycle, to increase the clock rate for other paths, and apply it to Furber's invention.

35. As per Claim 19, Furber and Hara teach: A method as claimed in claim 18, wherein adder logic used to perform said adding step is shared between the first address generation path and the at least one further address generation path (Hara, Column 19, Line 58 – Column 20, Line 4 discloses the adder, and Furber, Page 388

discloses that one path takes priority, meaning only one target can be output at a time, meaning the adder must be shared), but fails to explicitly teach:

the method further comprising the step of:

providing a pipeline stage in the at least one further address generation path in order to increase speed of generation of the target address by the first address generation path.

However, Patterson teaches that pipelining a processor, or adding stages of a pipeline, will reduce CPI, and reduce clock cycle time (increasing the rate at which the clock runs) (Page A-3), which would then speed up execution of the first address path, due to the increased clock rate. Given this advantage, it would have been obvious to one of ordinary skill in the art at the time the invention was made to pipeline a processing path that took one long clock cycle, to increase the clock rate for other paths, and apply it to Furber's invention.

Conclusion

36. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

37. McMahan (USPN 5,692,168) teaches a prefetch buffer that detects change of flow instructions.

38. Oldfield et al. (United States Patent Application Publication 2003/0159019) teaches a prefetch buffer with a branch prediction unit to detect change of flow instructions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Fennema whose telephone number is (571) 272-2748. The examiner can normally be reached on Monday-Friday, 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Robert E Fennema
Examiner
Art Unit 2183

RF

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100